REMARKS

Claims 1-30 are pending. Applicants respectfully request reconsideration and reexamination of the application.

Claims 1-30 were provisionally rejected under the judicially created doctrine of double patenting over claims 1, 2, 5-12, 14-19, 21-24, and 26-30 of co-pending Application No. 10/629,221. Applicants are submitting with this response a terminal disclaimer for this pending application with respect to co-pending Application No. 10/629,221, which are commonly owned by Lattice Semiconductor Corporation. Therefore, Applicants respectfully request that the rejection under the judicially created doctrine of double patenting of Claims 1-30 be withdrawn.

Claims 1-3, 9-11, 17, 18, 20, and 26-29 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,622,208 to North [herein referred to as "North"].

North discloses a system-on-a-chip system with a soft cache (col. 2, lns. 55-65, abstract). A system clock generation scheme is illustrated in Fig. 9 having two PLLs 121 a,b that receive the on-chip 32.768 KHz oscillator 120 as a reference clock (col. 10, lns. 19-29). Thus, North discloses receiving by the PLLs 121 a,b or, more specifically, by prescalers 906 a,b, a standard reference clock signal, with

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP
2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

prescalers 906 a,b supporting the division of the reference clock by the values M1 and M2 prior to the inputs of PLLs 121 a,b, respectively (col. 10, lns. 24-41).

In contrast, in accordance with one or more embodiments of the present invention, a clock generator is disclosed that is able to receive input signals of various signal types (e.g., LVCMOS, LVTTL, SSTL, HSTL, LVDS, and LVPECL). Thus, North fails to teach or disclose "a first circuit adapted to programmably receive an input signal, having a possible range of voltage levels and signal types" as recited in Claim 1, "receiving an input signal, wherein the input signal may be a single-ended signal type or a differential signal type" as recited in Claim 17, or "programmably receiving input signals of various signal types and voltage levels and generating an input signal for a phase-locked loop" as recited in Claim 26.

Therefore, Applicants respectfully submit that Claims 1, 17, and 26 patentably distinguish over North and that corresponding dependent Claims 2, 3, 9-11, 18, 20, and 27-29 are also distinguishable for at least the same reasons. Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 102(e) of Claims 1-3, 9-11, 17, 18, 20, and 26-29 be withdrawn.

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

Claims 21, 23, 25, 26, and 28 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,690,224 to Moore [herein referred to as "Moore"].

Moore discloses a clock generating circuit and a programmable logic circuit (col. 1, lns. 30-40). A circuit is shown in Fig. 3 having a multiplexer block 222 adapted to receive and select one of the reference clock signals (e.g., REFCLK(N), where N is an integer) to provide to PLL 200 (col. 5, lns. 62-66, col. 4, lns. 41-56, col. 2, lns. 55-58). Thus, Moore discloses receiving and providing one of the standard reference clock signals to PLL 200.

In contrast, in accordance with one or more embodiments of the present invention, a clock generator is disclosed that is able to receive input signals of various signal types (e.g., LVCMOS, LVTTL, SSTL, HSTL, LVDS, and LVPECL). Thus, Moore fails to teach or disclose "an input circuit programmable to receive input signals of various signal types and voltage levels" as recited in Claim 21 or "programmably receiving input signals of various signal types and voltage levels and generating an input signal for a phase-locked loop" as recited in Claim 26.

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049

Therefore, Applicants respectfully submit that Claims 21 and 26 patentably distinguish over Moore and that corresponding dependent Claims 23, 25, and 28 are also

distinguishable for at least the same reasons. Therefore, Applicants respectfully request that the rejection under 35 U.S.C. § 102(e) of Claims 21, 23, 25, 26, and 28 be withdrawn.

Accordingly, Applicants respectfully submit that Claims 1-30 are in proper form for allowance. Reconsideration and withdrawal of the rejections are respectfully requested and a timely Notice of Allowance is solicited. If there are any questions regarding any aspect of the application, please call the undersigned at (949) 752-7040.

Certificate of Transmission

I hereby certify that this correspondence is being facsimile transmitted to the Commissioner for Patents, Fax No. 703-872-9306 on the date stated below.

Tina Kavanaugh October 8, 2004

Respectfully submitted,

Greg J. Michelson

Greg J. Michelson
Attorney for Applicant(s)
Reg. No. 44,940

LAW OFFICES OF
MACPHERSON KWOK
CHEN & HEID LLP

2402 Michelson Drive
SUITE 210
Irvine, CA 92612
(949) 752-7040
FAX (949) 752-7049